ABSTRACT OF THE DISCLOSURE

The instruction translator includes a translator for reading out a corresponding instruction from the instruction memory in response to the received address to be executed by the processor and translating the instruction in a second instruction architecture into an instruction in a first instruction architecture, an instruction cache for temporarily holding the instruction in the first instruction architecture after the translation by the translator in association with the address in the instruction memory, and a selector for searching the instruction cache in response to the received address of an instruction to be executed by the processor, and based on a determination result of whether or not an instruction corresponding to the instruction of the address is held in the instruction cache, selectively outputting an instruction output by the translator, and the corresponding instruction in the first instruction architecture which has been held in the instruction cache.